



CUSTOMER ADVISORY

ADV2105

Intel® Stratix® 10 Device H-Tile/L-Tile PCIe Update

Description:

Intel® is notifying customers of an important PCIe Express* update to the Intel® Stratix® 10 H-Tile/L-Tile devices. Refer to Table 1 for details and link to KDB article with recommendations and further actions.

Table 1

Update Details	Impacted software versions	KDB Article
<ul style="list-style-type: none">When using the Intel® L-tile and H-tile Avalon® Streaming and Avalon® Memory Mapped IP for PCI Express* in Gen3 Root Port mode, correctable errors or link down training may be observed due to sub-optimal preset bit settings for PCIe* Upstream Port (USP)/Downstream Port (DSP) Gen3 Root Port IP on both H tile and L tile.Permanent fix implemented in Intel® Quartus® Prime Pro Edition software ver20.3 and above.	All Intel Quartus Prime Pro Edition software ver20.2 and prior	Why does the Intel® L-tile and H-tile Avalon® Streaming and Avalon® Memory Mapped IP for PCI Express* observe correctable errors/link down train when operating in Gen3 Root Port mode?

Products Affected:

Impacted device families are Intel Stratix 10 H-Tile/L-Tile GX, MX, NX, SX, TX devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:

<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2105-opn-list.xlsx>

Change Implementation:

The permanent fix for the issue described in this customer advisory is available now. Refer to the relevant KDB link in Table 1.

Contact:

For more information, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:

<https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html>

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Revision History

Date	Rev	Description
03/31/2021	1.0.0	Initial Release

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